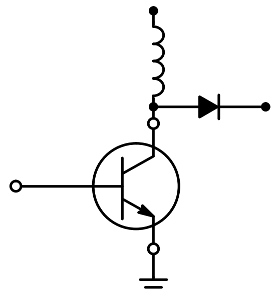
SWITCHMODE II Series
NPN Silicon Power Transistors

BUV48
BUV48A

The BUV48/BUV48A transistors are designed for high–voltage, high–speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line–operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

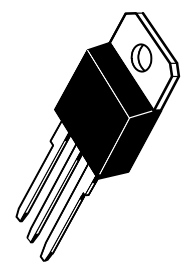


Fast Turn–Off Times
  60 ns Inductive Fall Time — 25°C (Typ)
  120 ns Inductive Crossover Time — 25°C (Typ)

Operating Temperature Range –65 to +175°C

100°C Performance Specified for:
  Reverse–Biased SOA with Inductive Loads
  Switching Times with Inductive Loads
  Saturation Voltage
  Leakage Currents (125°C)

15 AMPERES
NPN SILICON
POWER TRANSISTORS
400 AND 450 VOLTS
$V_{(BR)CEO}$
850 – 1000 VOLTS
$V_{(BR)CEX}$
150 WATTS



CASE 340D–01
TO–218 TYPE

MAXIMUM RATINGS

Rating	Symbol	BUV48	BUV48A	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	400	450	Vdc
Collector–Emitter Voltage (V_{BE} = –1.5 V)	V_{CEX}	850	1000	Vdc
Emitter Base Voltage	V_{EB}	7		Vdc
Collector Current — Continuous — Peak (1) — Overload	I_C I_{CM} I_{OI}	15 30 60		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	5 20		Adc
Total Power Dissipation — T_C = 25°C — T_C = 100°C Derate above 25°C	P_D	150 75 1		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +175		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

SWITCHMODE is a trademark of Motorola, Inc.

REV 7

MOTOROLA

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 200 mA, I_B = 0) L = 25 mH — BUV48 / BUV48A	$V_{CEO(sus)}$	400 450	— —	— —	Vdc
Collector Cutoff Current (V_{CEX} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEX} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	I_{CEX}	— —	— —	0.2 2	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEX}, R_{BE} = 10 Ω) — T_C = 25°C / T_C = 125°C	I_{CER}	— —	— —	0.5 3	mAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}	—	—	0.1	mAdc
Emitter–Base Breakdown Voltage (I_E = 50 mA – I_C = 0)	$V_{(BR)EBO}$	7	—	—	Vdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 10 Adc, V_{CE} = 5 Vdc) BUV48 (I_C = 8 Adc, V_{CE} = 5 Vdc) BUV48A	h_{FE}	8 8	— —	— —	
Collector–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2 Adc) (I_C = 15 Adc, I_B = 3 Adc) BUV48 (I_C = 10 Adc, I_B = 2 Adc, T_C = 100°C) (I_C = 8 Adc, I_B = 1.6 Adc) (I_C = 12 Adc, I_B = 2.4 Adc) BUV48A (I_C = 8 Adc, I_B = 1.6 Adc, T_C = 100°C)	$V_{CE(sat)}$	— — — — — —	— — — — — —	1.5 5 2 1.5 5 2	Vdc
Base–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2 Adc) BUV48 (I_C = 10 Adc, I_B = 2 Adc, T_C = 100°C) (I_C = 8 Adc, I_B = 1.6 Adc) BUV48A (I_C = 8 Adc, I_B = 1.6 Adc, T_C = 100°C)	$V_{BE(sat)}$	— — — —	— — — —	1.6 1.6 1.6 1.6	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	—	—	350	pF

SWITCHING CHARACTERISTICS
Resistive Load (Table 1)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Delay Time	I_C = 10 A, I_B, = 2 A BUV48 I_C = 8 A, I_B, = 1.6 A BUV48A Duty Cycle ≤ 2%, $V_{BE(off)}$ = 5 V T_p = 30 µs, V_{CC} = 300 V	t_d	—	0.1	0.2	µs
Rise Time		t_r	—	0.4	0.7	
Storage Time		t_s	—	1.3	2	
Fall Time		t_f	—	0.2	0.4	

Inductive Load, Clamped (Table 1)

Characteristic	Conditions		Symbol	Min	Typ	Max	Unit
Storage Time	I_C = 10 A, I_{B1} = 2 A BUV48	(T_C = 25°C)	t_{sv}	—	1.3	—	µs
Fall Time			t_{fi}	—	0.06	—	
Storage Time	I_C = 8 A, I_{B1} = 1.6 A BUV48A	(T_C = 100°C)	t_{sv}	—	1.5	2.5	
Crossover Time			t_c	—	0.3	0.6	
Fall Time			t_{fi}	—	0.17	0.35	

(1) Pulse Test: Pulse Width = 300 µs, Duty Cycle ≤ 2%.
Vcl = 300 V, $V_{BE(off)}$ = 5 V, Lc = 180 µH

DC CHARACTERISTICS

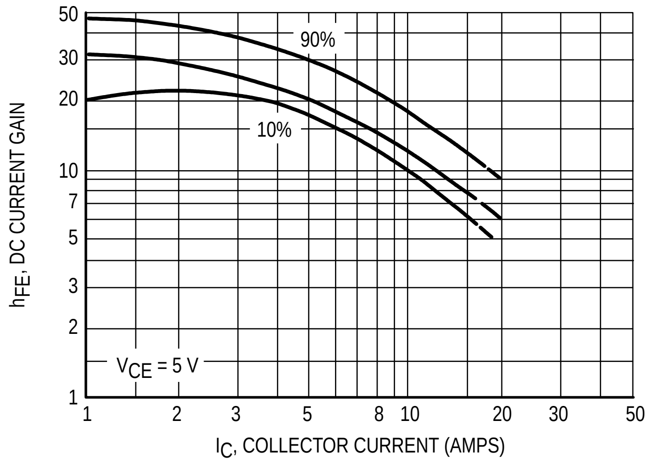


Figure 1. DC Current Gain

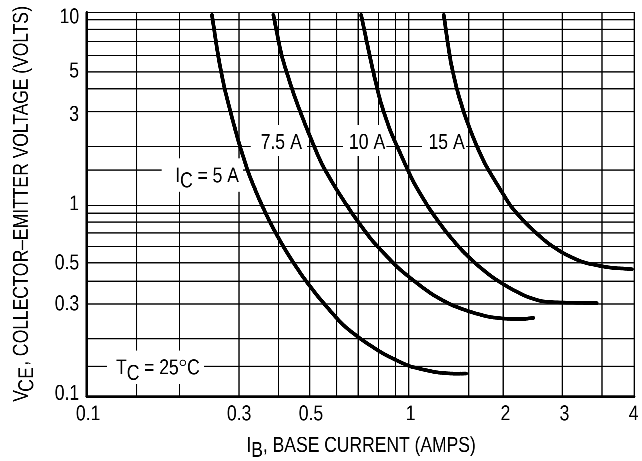


Figure 2. Collector Saturation Region

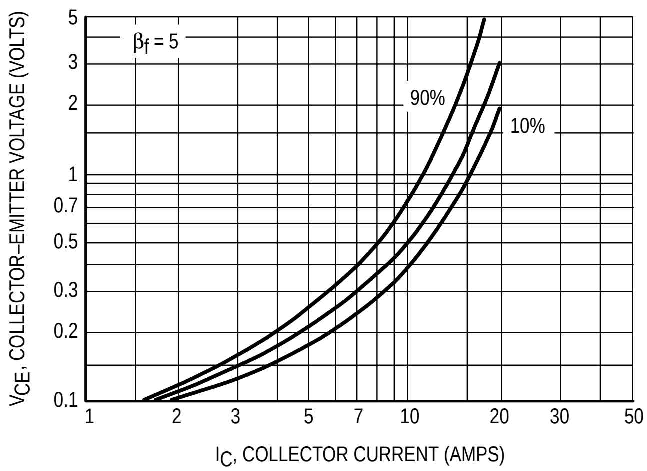


Figure 3. Collector–Emitter Saturation Voltage

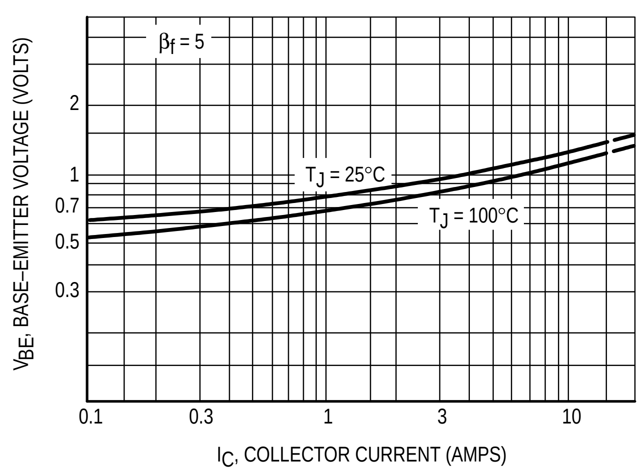


Figure 4. Base–Emitter Voltage

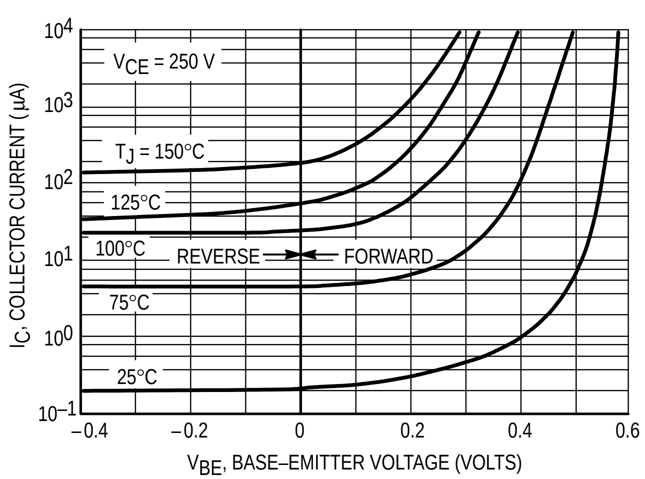


Figure 5. Collector Cutoff Region

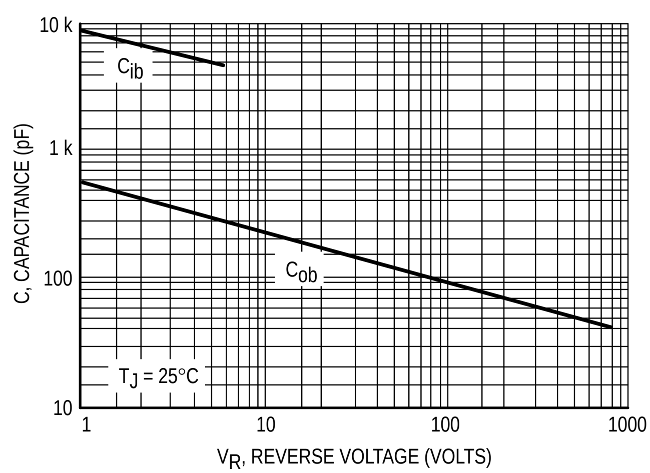
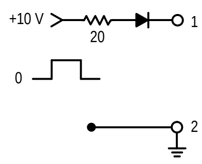
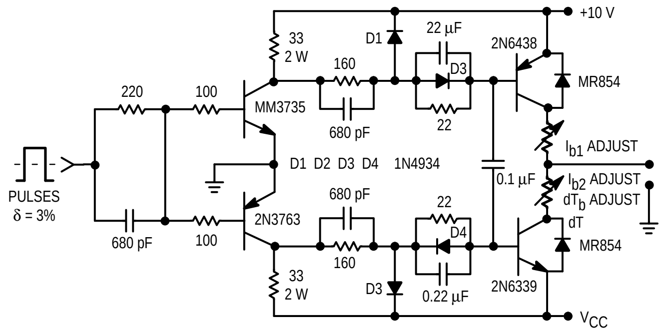
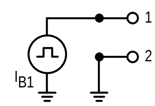
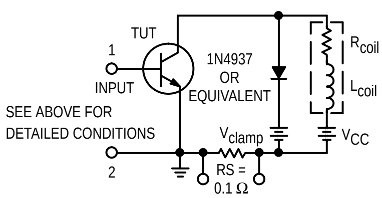
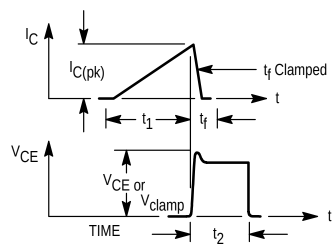
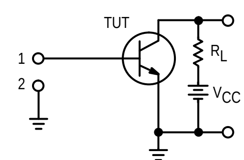


Figure 6. Capacitance

Table 1. Test Conditions for Dynamic Performance

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 200 mA		**TURN–ON TIME**  I_{B1} adjusted to obtain the forced h_{FE} desired **TURN–OFF TIME** Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 25 mH, V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 300 V R_B ADJUSTED TO ATTAIN DESIRED I_{B1}	V_{CC} = 300 V R_L = 83 Ω Pulse Width = 10 µs
TEST CIRCUITS	**INDUCTIVE TEST CIRCUIT** 	**OUTPUT WAVEFORMS**  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{Clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	**RESISTIVE TEST CIRCUIT** 

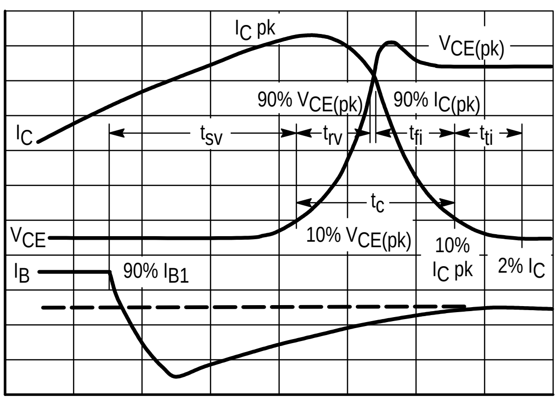


Figure 7. Inductive Switching Measurements

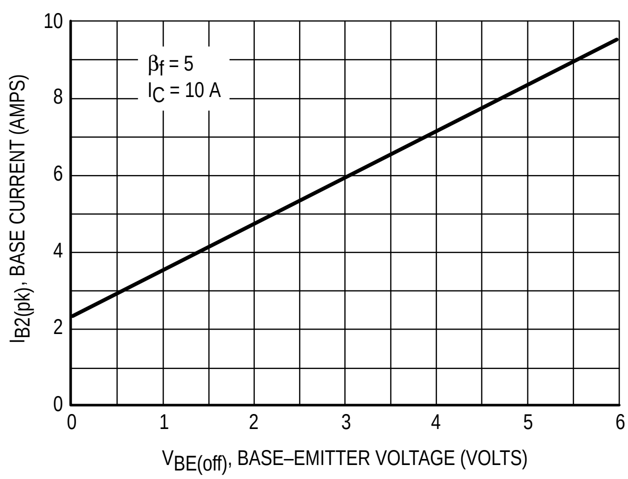


Figure 8. Peak–Reverse Current

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

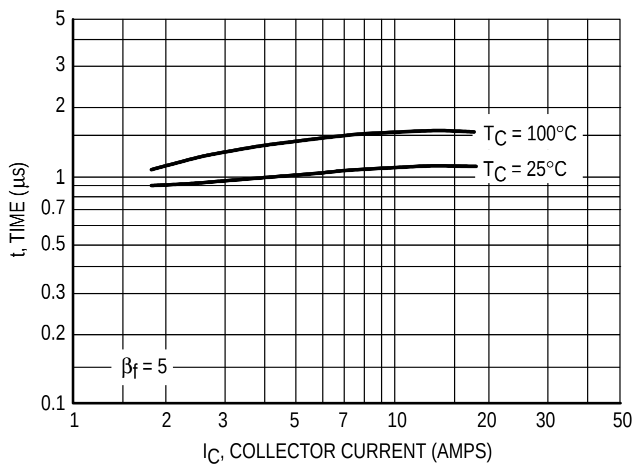


Figure 9. Storage Time, t_{sv}

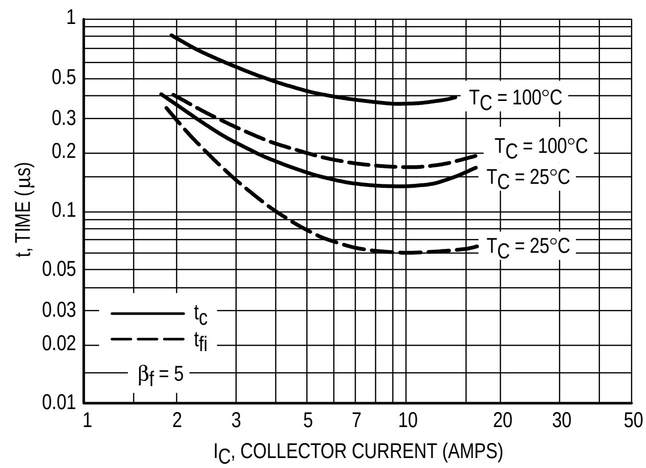


Figure 10. Crossover and Fall Times

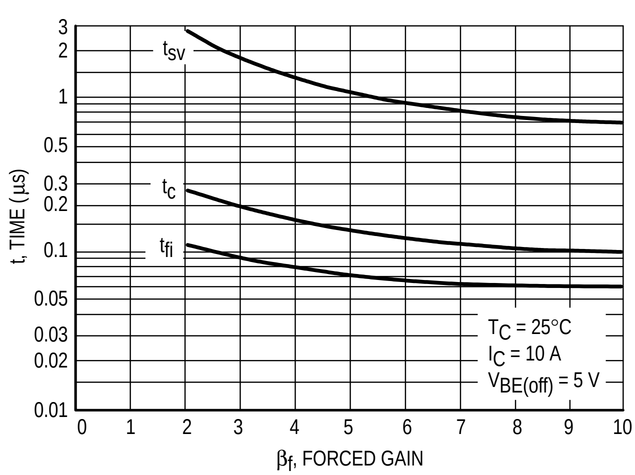


Figure 11a. Turn–Off Times versus Forced Gain

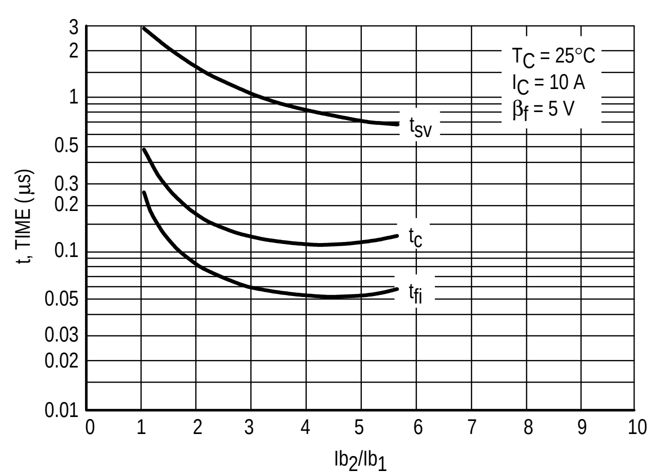


Figure 11b. Turn–Off Times versus Ib_2/Ib_1

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

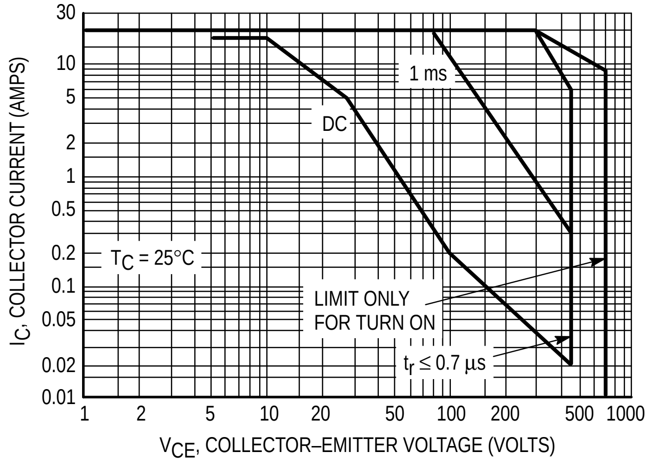


Figure 12. Forward Bias Safe Operating Area

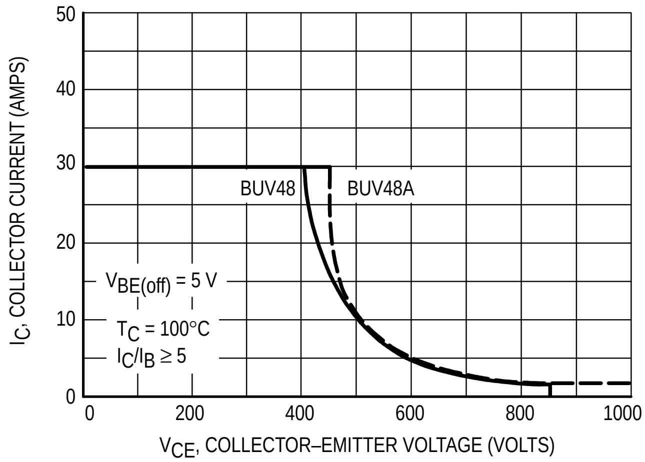


FIgure 13. Reverse Bias Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \le$ 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage current conditions during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

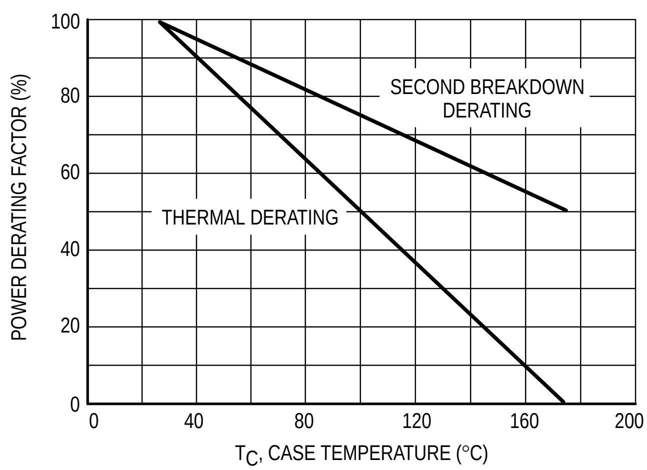


Figure 14. Power Derating

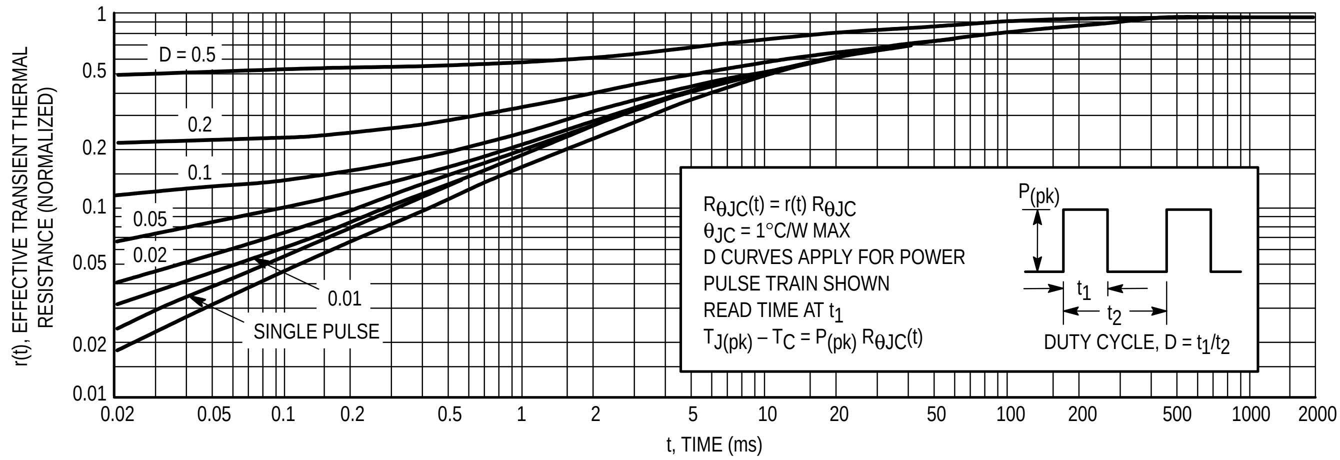


Figure 15. Thermal Response

OVERLOAD CHARACTERISTICS

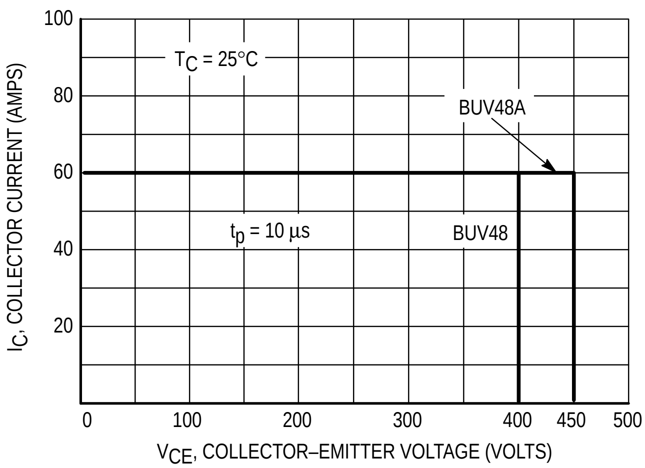


Figure 16. Rated Overload Safe Operating Area (OLSOA)

OLSOA

OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known.

Maximum allowable collector–emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

OLSOA is measured in a common–base circuit (Figure 18) which allows precise definition of collector–emitter voltage and collector current. This is the same circuit that is used to measure forward–bias safe operating area.

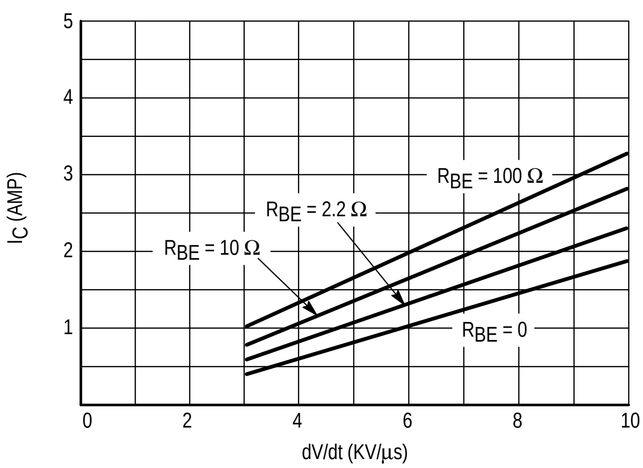


Figure 17. I_C = f(dV/dt)

Notes:
- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p

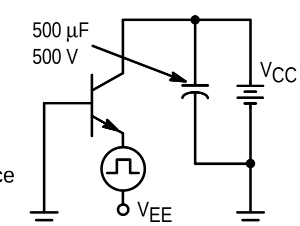
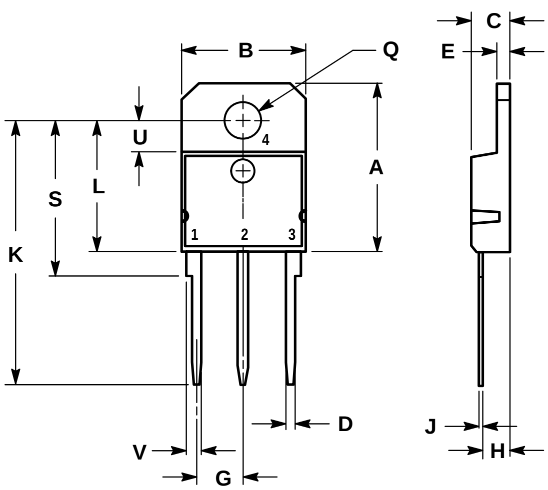


Figure 18. Overload SOA Test Circuit

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.00	19.60	0.749	0.771
B	14.00	14.50	0.551	0.570
C	4.20	4.70	0.165	0.185
D	1.00	1.30	0.040	0.051
E	1.45	1.65	0.058	0.064
G	5.21	5.72	0.206	0.225
H	2.60	3.00	0.103	0.118
J	0.40	0.60	0.016	0.023
K	28.50	32.00	1.123	1.259
L	14.70	15.30	0.579	0.602
Q	4.00	4.25	0.158	0.167
S	17.50	18.10	0.689	0.712
U	3.40	3.80	0.134	0.149
V	1.50	2.00	0.060	0.078

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 340D–01
TO–218 TYPE
ISSUE A

How to reach us:
USA / EUROPE: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE (602) 244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, Toshikatsu Otsuki,
6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298